Abstract

A semiconductor package (1; 18; 20) comprises a substrate (3; 21) and a semiconductor chip (2) which includes an active surface with a plurality of chip contact areas (13). The chip (2) is electrically connected to the substrate (3; 21). The substrate comprises a sheet of core material (5), a plurality of upper conducting traces (6) and upper contact pads (7) on its upper surface, a second plurality of lower conductive traces (8) and external contact areas (9) on its bottom surface. A plurality of conducting vias (10) connect the conducting traces (6) and lower conducting traces (8). The substrate (3; 21) also includes a plurality of vent holes (4; 22) and a layer of solder resist (15) covering the upper and lower surfaces of the substrate (3) leaving the contact areas (6 and 8) free from solder resist (15).

[Fig. 1]